U.S. patent application serial number 10/045,821 by T. B. Berg et al. (BEA920000018US1) entitled "Multi-level Classification Method For Transaction Address Conflicts For Ensuring Efficient Ordering In A Two-level Snoopy Cache Architecture" was filed on January 9, 2002.

U.S. patent application serial number 10/045,564 by S.G. Lloyd et al. (BEA920000019US1) entitled "Transaction Redirection Mechanism For Handling Late Specification Changes And Design Errors" was filed on January 9, 2002.

U.S. patent application serial number 10/045,797 by T. B. Berg et al. (BEA920000020US1) entitled "Method And Apparatus For Multi-path Data Storage And Retrieval" was filed on January 9, 2002.

U.S. patent application serial number 10/045,925 by T. B. Berg et al. (BEA920000022US1) entitled "Distributed Allocation Of System Hardware Resources For Multiprocessor Systems" was filed on January 9, 2002.

U.S. patent application serial number 10/045,926 by W. A. Downer et al. (BEA920010030US1) entitled "Masterless Building Block Binding To Partitions" was filed on January 9, 2002.

U.S. patent application serial number 10/045,774 by W. A. Downer et al. (BEA920010031US1) entitled "Building Block Removal From Partitions" was filed on January 9, 2002.

U.S. patent application serial number 10/045,796 by W. A. Downer et al. (BEA920010041US1) entitled "Masterless Building Block Binding To Partitions Using Identifiers And Indicators" was filed on January 9, 2002.

In the Claims

Please amend claim 1 to read in full as follows:

1. (Amended) A multiprocessor computer system comprising:

first, second and other processing nodes, each including at least one processor;

a communication pathway connecting said nodes and including a central hardware device;

a shared, distributed system memory, a portion of said shared system memory being coupled to said processors and to said communication pathway; and